

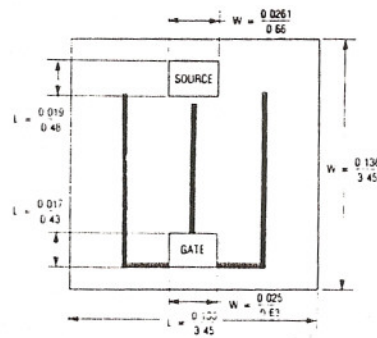


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

D22



HEX-2: 800 to 1000V,
 N-Channel

Topside Metal: Al
Backside: CrNiAg
Backside Potential: Drain
Mask Ref: Issue 1
Bond Pads: .003" min

APPROVED BY: CB
MFG: IRI

DIE SIZE: .136" x .136"
THICKNESS: .019"

DATE: 2/8/01
P/N: IRFCG20

DG 10.1.2
 Rev A 3-4-99